In addition to a reduced oxygen to silane ratio, the method of the present invention allows for low etch-to-deposition (E/D) ratios, corresponding to greater gap-fill capability. An E/D ratio is defined by the equation:

E/D = (UBUC-BUC)/UBUC

where UBUC is the deposition rate of the process with no wafer bias or clamping (unbiased, unclamped) and no gas flow change as compared to the BUC process, and BUC is the deposition rate of the process with wafer bias and no clamping (biased, unclamped). In one embodiment of the present invention, as the minimized oxygen to silane ratio is used to minimize the oxygen flow rate and to reduce the silane flow rate for depositing a dielectric layer, E/D ratios have also been reduced. Reduced E/D ratios correspond to the overall sputtering rate decreasing, and the aspect ratio gapfill capability increasing. For example, E/D ratios from about 0.0 to about -0.05 have been achieved for void-free gap filling, where the UBUC-deposited film refractive index ranges from about 1.5 to about 1.6 and the BUC-deposited film refractive index is about 1.46.

IN THE CLAIMS

The following is a clean version of the amended claims. In accordance with 37 C.F.R. §1.121(c)(2)(ii), Attachment B provides marked-up versions of the claims containing the newly introduced changes. Please amend Claims 1, 11, 12, 14-16, and 19 as indicated. Claim 30 has been added.

1. (Amended) A method for filling a gap during integrated circuit fabrication, comprising:

providing a gas mixture comprised of a silicon-containing component and an oxygen-containing component; and

performing an HDP-CVD process using the gas mixture to fill the gap with a dielectric, wherein the ratio of the oxygen-containing component to the silicon-containing component is substantially the minimum necessary to form the dielectric.

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